L Number	Hits	Search Text	DB	Time stamp
4	2584	undoped with (silicon silicate) with	USPAT;	2004/03/19
5	12740	oxide usg phosphosilicate with glass psg	EPO; JPO USPAT; EPO; JPO	10:31 2004/03/19 10:32
6	16603	sion (silicon silicate) with oxynitride	USPAT; EPO; JPO	2004/03/19
7	199	(undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)	USPAT; EPO; JPO	2004/03/19 10:33
9	9	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and integrated adj circuit and active with (area region) and plug\$4 and metal adj layer	USPAT; EPO; JPO	2004/03/19 14:57
10	1	6492224.pn.	USPAT; EPO; JPO	2004/03/19 11:03
11	1	6144060.pn.	USPAT; EPO; JPO	2004/03/19 11:03
15	1	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and integrated adj circuit and active with (area region) and solder\$4 and etch\$3 and polyimide and metal adj layer	USPAT; EPO; JPO	2004/03/19 15:50
16	2	("5220199" "6037668").PN.	USPAT	2004/03/19 15:28
17	9	6232662.URPN.	USPAT	2004/03/19 15:29
35	1	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and integrated near3 circuit and active with (area region) and solder\$4 and etch\$3 and polyimide and metal adj layer	USPAT; EPO; JPO	2004/03/19 15:50
36	1		USPAT; EPO; JPO	2004/03/19 15:51
37	8	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and active with (area region) and (connect connecting connection) and etch\$3 and polyimide and metal adj layer	USPAT; EPO; JPO	2004/03/19 17:11
40			USPAT; EPO; JPO	2004/03/19 17:13
41	4		USPAT; EPO; JPO	2004/03/19 17:16
42	0	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxynitride)) and 29/\$.ccls.	USPAT; EPO; JPO	2004/03/19 17:17
43	158	((undoped with (silicon silicate) with oxide usg) and (phosphosilicate with glass psg) and (sion (silicon silicate) with oxymitride)) and 257/\$.ccls.	USPAT; EPO; JPO	2004/03/19 17:17

		[/ / / d /	TICDAM .	2004/02/10
44	8	, , , ,	USPAT;	2004/03/19
		oxide usg) and (phosphosilicate with	EPO; JPO	17:18
		glass psg) and (sion (silicon silicate)		
		with oxynitride)) and 257/\$.ccls.) and		
		metal adj pad	HCDAM.	2004/02/18
_	1	redistribution.ti. and danielle.in.	USPAT;	2004/03/18
			US-PGPUB;	17:16
İ	1	1 . 11 . t 11	EPO; JPO	2004/02/10
-	17	redistribution adj layer and plug	USPAT;	2004/03/18
	2224		EPO; JPO	18:04
-	3774	active with circuit with area	USPAT;	2004/03/18
Ì	00.60		EPO; JPO	17:20
-	2362		USPAT;	2004/03/18
		integrated adj circuit	EPO; JPO	17:21
-	577		USPAT;	2004/03/18 17:21
		integrated adj circuit) and metal adj	EPO; JPO	17:21
	405	layer	IICDAM.	2004/02/18
_	405		USPAT;	2004/03/18
	1	integrated adj circuit) and metal adj	EPO; JPO	17:22
	225	layer) and connect\$3 and etch\$3	HCDAT.	2004/02/19
_	235	` ` ` ` · · · · · · · · · · · · · · ·	USPAT; EPO; JPO	2004/03/18 17:29
		integrated adj circuit) and metal adj layer) and connect\$3 and etch\$3) and	PEC, OEC	11.63
]	silicon with oxide		
_	10	Silicon with oxide ((((active with circuit with area) and	USPAT;	2004/03/18
-	19	integrated adj circuit) and metal adj	EPO; JPO	17:39
	ĺ	layer) and connect\$3 and etch\$3) and	TEO, UPO	11.39
		silicon with oxide) and glass adj layer	•	
		and substrate		
	o		USPAT;	2004/03/18
-	١ ٠	adj layer and undoped with silicon and	EPO; JPO	17:41
		polyimide and etch\$3 and connect\$3 and	Bro, oro	17.31
		metal adj layer		
_	22		USPAT;	2004/03/18
	22	with layer and oxide with silicon and	EPO; JPO	17:42
		polyimide and etch\$3 and connect\$3 and	210, 010	1,,,,,
		metal adj layer		
_	3	,	USPAT;	2004/03/18
}		circuit with area)	EPO; JPO	18:05
_	9	redistribution with (film layer) and	USPAT;	2004/03/18
	_	(active with circuit with area)	EPO; JPO	18:14
_	1632	undoped with silicon with oxide	USPAT;	2004/03/18
		•	EPO; JPO	18:40
_	4223	phosphosilicate with glass	USPAT;	2004/03/18
			EPO; JPO	18:41
-	7474	silicon with oxynitride	USPAT;	2004/03/18
			EPO; JPO	18:41
-	76	(undoped with silicon with oxide) and	USPAT;	2004/03/18
		(phosphosilicate with glass) and (silicon	EPO; JPO	18:16
		with oxynitride)		
-	30	((undoped with silicon with oxide) and	USPAT;	2004/03/18
		(phosphosilicate with glass) and (silicon	EPO; JPO	18:17
		with oxynitride)) and plug\$3		
-	30		USPAT;	2004/03/18
		(phosphosilicate with glass) and (silicon	EPO; JPO	18:19
1		with oxynitride)) and plug\$4		
-	55	, , ,	USPAT;	2004/03/18
1		(phosphosilicate with glass) and (silicon	EPO; JPO	18:20
1		with oxymitride)) and (ic chip integrated		
		adj circuit)		
-	2541	(undoped with silicon with oxide) usg	USPAT;	2004/03/18
			EPO; JPO	18:40
-	13084	(phosphosilicate with glass) bpsg	USPAT;	2004/03/18
			EPO; JPO	18:41
-	16545	(silicon with oxynitride) sion	USPAT;	2004/03/18
			EPO; JPO	18:41
-	6	((undoped with silicon with oxide) usg)	USPAT;	2004/03/18
1	1	and ((phosphosilicate with glass) bpsg)	EPO; JPO	18:43
		and ((silicon with oxynitride) sion) and		
	1	integrated adj circuit and active with		
	L	circuit with (area region) and plug\$4		
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	U	1	D	ocument	ID	Issue Date	Pages	Title	Current OR	Curren
30	П	P		6483150		20021119	11	Semiconductor device with both memories and logic	257/368	257/E2 257/E2
31	Г	17				20020730	16	Reliable metal bumps on top of I/O pads with test probe	257/738	257/76
32		•	(20010918	13	Method and structure to make planar analog capacitor on		257/E2 257/E2
33	П					20010814	13	Capacitor electrode having conductive regions adjacent	257/298	257/30 257/30
34		M					17	Process for fabricating vertical transistors	438/268	257/E2 257/E2
35	П		1			20000912	10	Method of forming contact plugs in a semiconductor	438/637	257/E2 257/E2
36	Г	Þ	បន	6100202	A	20000808	15	Pre deposition stabilization method for forming a void	438/734	257/E2 257/E2
37	С	17.		6037220		20000314	13	Method of increasing the surface area of a DRAM	438/255	257/E2 257/E2
38			•			20000222	15	Process for fabricating vertical transistors	438/268	257/E2 257/E2
39	П		ì				15	Ferroelectric capacitors on protruding portions of	257/295	257/30
40		Þ	បទ	6238968	В1	20010529	17	Methods of forming integrated circuit	438/253	257/E2 438/25
41		F					10	System and method for bonding over active	257/750	257/73 257/E2
42	П						12	CMP process utilizing dummy plugs in damascene process	438/692	438/62 438/62
43	П						7	Method of making a dielectric structure for	438/624	257/E2 257/E2
44		F	US	4990464	A	19910205	4	Method of forming improved encapsulation layer	117/43	117/90 148/DI

US 6166444 A		257/777	257/777 Hsuan, Min-Chih et al.
US 20030167632	20030911 System and method for providing a redistribution metal layer in an integrated circuit	29/841	Thomas, Danielle A. et a
US 6060355 A	20000509 Process for improving roughness of conductive layer	438/255	
US 5770500 A	19980623 Process for improving roughness of conductive layer	438/255	Batra, Shubneesh et al.
US 6677613 B1	20040113 Semiconductor device and method of fabricating the same	257/72	Yamazaki, Shunpei et al.
US 6661057 B1	Tri-level segmented control transistor	257/336	Dawson, Robert et al.
US 6650002 B1	20031118 Semiconductor device having active element connected to an electrode metal pad via a barrier metal 1257/637	1257/637	Toyosawa, Kenji et al.
US 6620656 B2	20030916 Method of forming body-tied silicon on insulator semiconductor device	438/149	438/149 Min, Byoung W. et al.
US 6548392 B2	20030415 Methods of a high density flip chip memory arrays	438/612	Akram, Salman et al.
US 6472244 B1	20021029 Manufacturing method and integrated microstructures of semiconductor material and integrated piezore438/53	re438/53	Ferrari, Paolo et al.
US 6455424 B1	20020924 Selective cap layers over recessed polysilicon plugs	438/675	438/675 McTeer, Allen et al.
US 6432809 B1	20020813 Method for improved passive thermal flow in silicon on insulator devices	438/618	Tonti, William R. et al.
US 6441467 B2	20020827 Semiconductor device having active element connected to an electrode metal pad via a barrier metal 1257/637	1257/637	Toyosawa, Kenji et al.
US 6384486 B2	20020507 Bonding over integrated circuits	257/781	Zuniga, Edgar R. et al.
US 6348709 B1	20020219 Electrical contact for high dielectric constant capacitors and method for fabricating the same	257/311	Graettinger, Thomas M.
US 6174735 B1	20010116 Method of manufacturing ferroelectric memory device useful for preventing hydrogen line degradation	า 438/3	Evans, Thomas A.
US 5972774 A	19991026 Process for fabricating a semiconductor device having contact hole open to impurity region coplanar w/438/435	wi438/435	Matumoto, Akira
US 5939790 A	19990817 Integrated circuit pad structures	257/773	
US 5895239 A	19990420 Method for fabricating dynamic random access memory (DRAM) by simultaneous formation of tungster 438/239	er#38/239	
US 5719416 A	19980217 Integrated circuit with layered superlattice material compound	257/295	
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US 5815223 A	19980929 Display device having a silicon substrate, a locos film formed on the substrate, a tensile stress film form849/42	rrf849/42	
US 6461895 B1	20021008 Process for making active interposer for high performance packaging applications	438/107	Liang, Chunlin et al.
US 5106769 A	19920421 Process for manufacturing bi-cmos type semiconductor integrated circuit	438/207	Matsumi, Koji
US 6649508 B1	20031118 Methods of forming self-aligned contact structures in semiconductor integrated circuit devices	438/618	_
US 6635536 B2	20031021 Method for manufacturing semiconductor memory device	438/276	
US 6605510 B2		438/275	
US 6600187 B2		257/296	Kim, Jeong-Seok
US 6483150 B1	20021119 Semiconductor device with both memories and logic circuits and its manufacture	257/368	257/368 Watatani, Hirofumi
US 6426556 B1	20020730 Reliable metal bumps on top of I/O pads with test probe marks	257/738	Lin, Mou-Shiung
US 6410424 B1	20020625 Process flow to optimize profile of ultra small size photo resist free contact	438/637	Tsai, Ming-Huan et al.
US 6300250 B1	20011009 Method of forming bumps for flip chip applications	438/694	
6291307	20010918 Method and structure to make planar analog capacitor on the top of a STI structure	438/393	Chu, Shao-Fu Sanford et
US 6274899 B1	20010814 Capacitor electrode having conductive regions adjacent a dielectric post	257/298	Melnick, Bradley M. et al
US 6197641 B1	20010306 Process for fabricating vertical transistors	438/268	438/268 Hergenrother, John Mich

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US 6117766 A	US 6117766 A 20000912 Method of forming contact plugs in a semiconductor device	438/637	438/637 Yoon, Bo-Un et al.	-
US 6100202 A	20000808 Pre deposition stabilization method for forming a void free isotropically etched anisotropically patterned438/734 Lin, Been-Hon et al.	d438/734	Lin, Been-Hon et al.	
US 6037220 A	US 6037220 A 20000314 Method of increasing the surface area of a DRAM capacitor structure via the use of hemispherical grain438/255 Chien, Ho-Ching et al.	n438/255	Chien, Ho-Ching et al.	
US 6027975 A	US 6027975 A 20000222 Process for fabricating vertical transistors	438/268	438/268 Hergenrother, John M. et	ह्रा
US 6576941 B1	US 6576941 B1 20030610 Ferroelectric capacitors on protruding portions of conductive plugs having a smaller cross-sectional siz 257/295 Lee, Moon-Sook et al.	:257/295	Lee, Moon-Sook et al.	
US 6238968 B1	US 6238968 B1 20010529 Methods of forming integrated circuit capacitors having protected layers of HSG silicon therein	438/253	438/253 Yu. Young-Sub et al.	

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